REMARKS

The Applicants respectfully request reconsideration and allowance of claims 1-18 in view of the following arguments. The Applicants appreciate the Examiner finding the arguments of the previous response persuasive.

INTERVIEW SUMMARY

The Applicants appreciate the telephone interview conducted April 21, 2005, between Examiner Sharon and Applicants' attorney, Russell Scott. In the interview, the Applicants' attorney summarized the arguments presented below and emphasized the fundamental distinctions between the Avidan patent (U.S. Patent No. 6,158,022) and Applicants' claims. The general difference between Avidan and Applicants' claims were discussed as well as some of the particular differences between the static timing analysis of Applicants' claims and the analysis conducted in Avidan. Specifically, Avidan's failure to use circuit simulation to determine timing characteristics for creating a timing model was discussed. No agreement was reached as to the allowability of the claims.

CLAIMS 1-18 ARE NOT ANTICIPATED BY THE CITED PRIOR ART

The Examiner rejected claims 1-18 under 35 U.S.C. § 102(e) as being anticipated by Avidan. The Applicants respectfully submit that the claims are not anticipated by this reference.

<u>The Foltin Reference</u>

The Examiner refers to Foltin to support the Section 102 rejection of claims 1-18. However, in the detailed analysis, the Examiner actually combined the express teachings in

Avidan with belated interpretative teachings, as interpreted by Foltin, as the basis for the Section 102 rejection. The Applicants' submit that the Examiner's reliance on Foltin's interpretation of the Avidan reference is clearly improper under 35 U.S.C. §102. If Avidan actually taught the invention, interpretation by Foltin would be unnecessary. Furthermore, neither Avidan nor Foltin's interpretation of Avidan discloses performing a circuit simulation to determine timing characteristics as recited in Applicants' claims.

The Avidan Patent

Avidan discloses a circuit analyzer of circuits containing black box, gray box, and transparent elements (Avidan, col. 2, lines 55-56). With these elements, the design engineer need not convert to a device-level model or regenerate a timing model to verify a design (Avidan, col. 3, lines 13-14).

The Avidan Patent Fails to Teach Each Element Required in the Respective Claims

Applicants' independent claim 1 is directed to a method for analyzing an electronic circuit and requires the following method steps:

(a) replacing at least one timing determinant block in a first functional component of the circuit with a timing element set;
(b) performing a circuit simulation for a cross-section of the first functional component to determine timing characteristics associated with each replaced timing determinant block of the first functional component;
(c) attaching the timing characteristics associated with each replaced timing determinant block to the respective timing element set which replaced the respective timing determinant block, thereby creating a timing model for the first functional component; and
(d) performing a static timing analysis for the circuit utilizing the timing model for the first functional component.

Applicants respectfully submit that Avidan fails to teach, suggest, or otherwise disclose performing a circuit simulation for a cross-section of a first functional component of a circuit to determine timing characteristics associated with each replaced timing determinant block of the first functional component as required in element (b) of Applicants' claim 1. Also, nothing in Avidan discloses or suggests performing a static timing analysis using the timing model defined in claim 1 as required by element (d) of claim 1.

Further, although the timing model of Applicants' claims may be considered to be a type of gray box, Applicants' gray box is different from the gray box disclosed in Avidan because Applicants' gray box is created from the timing characteristics determined by performing the circuit simulation for the cross-section of the first functional component of the circuit to be analyzed. Significantly, Avidan fails to disclose performing a circuit simulation to determine timing characteristics.

For the above reasons the Avidan reference fails to teach or suggest all of the elements required in claim 1. Thus, Applicants urge the Examiner to withdraw the §102 rejection of independent claim 1 as being anticipated by Avidan. The Examiner is also urged to withdraw the §102 rejection of claims 2-7, which depend from claim 1.

Regarding, Applicants' independent claims 8 and 14, Applicants respectfully submit that these claims recite limitations analogous to those found in independent claim 1. For example, claims 8 and 14 each include the limitations of replacing at least one timing determinant block in a functional component of a circuit with a timing element set, performing a circuit simulation for a cross-section of the functional component to determine timing characteristics associated with each replaced timing determinant block of the functional component, and attaching the timing characteristics associated with each replaced timing determinant block to the respective timing

element set which replaced the respective timing determinant block. Thus, the arguments presented above with respect to claim 1 apply with equal force to independent claims 8 and 14. The Examiner is therefore urged to withdraw the §102 rejection of independent claims 8 and 14 and their respective dependant claims.

CONCLUSION

For all of the above reasons, the Applicants respectfully request reconsideration and allowance of claims 1-18.

If any issue remains as to the allowability of these claims, or if a conference might expedite allowance of the claims, the Examiner is asked to telephone the undersigned attorney prior to issuing a further action in this case.

Respectfully submitted,

THE CULBERTSON GROUP, P.C.

Dated: 6 July 2005

By: _____

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CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax No. 703-872-9306) on July 6, 2005.

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